Using SolidWorks & COSMOS/Works for MEMS Designs

Abstract

In this application example, we present a simple MEMS design executed with SolidWorks. We then analyze some of the performance and reliability considerations for the modeled structure acting as an electrostatically deflected mirror array, using COSMOS/Works to estimate deflection *vs*. voltage and the resulting stresses. We suggest approaches to deal with the physics of very small structures as appropriate to modeling MEMS devices with finite element analysis (FEA).

Finally, we demonstrate the generation of a two-dimensional mask layout from a three-dimensional solid model. The mask layout may be used to produce a photomask for contact printing or projection in a mask aligner. The sample MEMS design comprises an array of nickel mirror elements created with bulk micromachining. The nickel mirror elements are patterned on a silicon base in a fashion suggested by Parameswaran, *et al.*[1]

Design Considerations

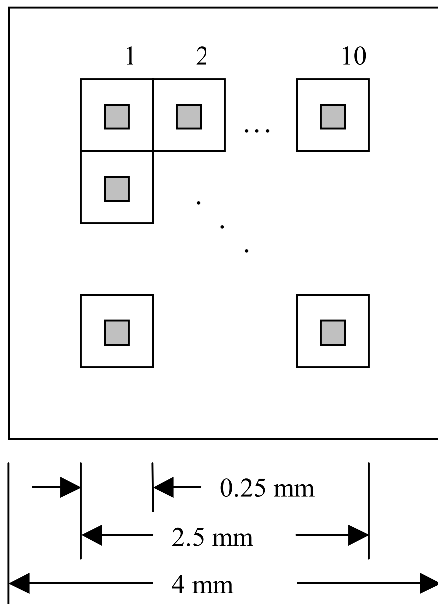

Figure 1. A 10 x 10 array of MEMS mirrors, patterned on 250 µm centers. In this schematic view, the gray regions represent the desired mirrors.

For this example, we construct a MEMS array with mirror elements that are 50 µm x 50 µm, where the unit cell is 250 µm square. The mirror element size was chosen to easily handle 20 µm diameter optical beams, providing margin for misalignment.

We demonstrate the design of a square array comprising 100 elements. This geometry is sketched in Figure 1, where we have omitted detail within each unit cell for clarity. The active region within each die is 2.5 mm x 2.5 mm and each die is a square, 4 mm on a side. Figure 2 demonstrates that a typical 8 inch silicon wafer could produce approximately 1,200 dies.

The bulk micromachining process can be accomplished with the following procedure:

- deposit and softbake positive photoresist over a <100>* Si wafer
- expose the photoresist with the mask aligned to the <110> direction
- develop and hardbake the photoresist
- deposit nickel to desired thickness†
- strip photoresist
- anneal
- anisotropic etch

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* Crystal plane orientations are designated inside carets "< >" to avoid confusion with numerical quantities.

† One goal of the COSMOS/Works evaluation is comparison of the performance of a 1 µm Ni layer, achieved with sputter deposition and patterned with metal lift-off techniques, *vs*. a 5 µm thickness electroless Ni plating, which only plates to bare Si. The process described here assumes electroless plating.

Positive photoresist is removed in the exposed regions upon development. Therefore, exposed regions will be bare silicon, which will be directly coated with nickel. After photoresist removal, the anisotropic etch will etch along the <111> crystal planes, resulting in a sidewall angle of 54.74º with the surface.

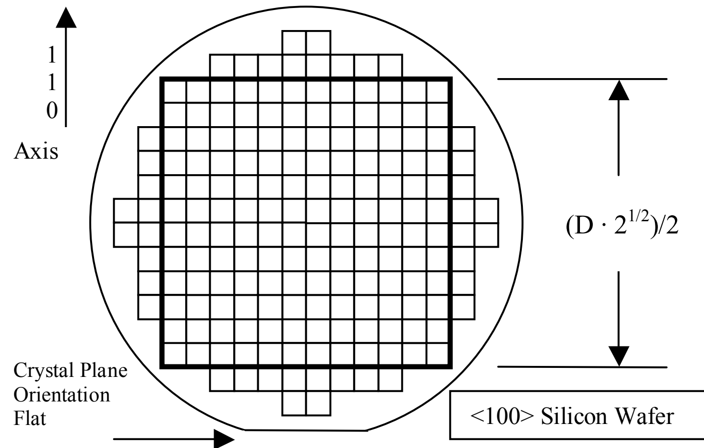

Figure 2. The arrangement of dies on a wafer. For an eight-inch wafer, the side of the square is approximately 140 mm, producing an array of 35 x 35 dies (only 12 x 12 shown).

The mask needed for this example will let light through only where nickel is desired. The mask should therefore be opaque in the area surrounding the desired nickel pattern. Figure 3 illustrates the unit cell of nickel that should be left behind, indicated as the dark portions of the diagram. Figure 4 is an example of the positive mask needed to produce the same shape. In this diagram, the white portions are transparent and will therefore result in the absence of photoresist upon development, yielding nickel deposits. During the anisotropic silicon etch step, the silicon directly beneath the portions that are opaque in Figure 4 will be exposed to the etchant.

Figure 3. Unit cell nickel pattern.

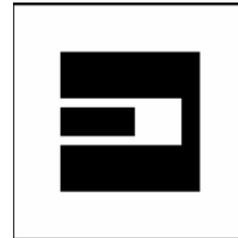

Figure 4. Unit cell photoresist pattern.

Modeling the MEMS Structure

The unit mirror structure was designed to produce a significant deflection with relatively low force loading. The active area ratio is thus approximately 4 %, due to the long suspension arms. The 250 mm unit cell dimension is appropriate to commonly available lens arrays. Figure 5 details the dimensions chosen for the first-pass design.

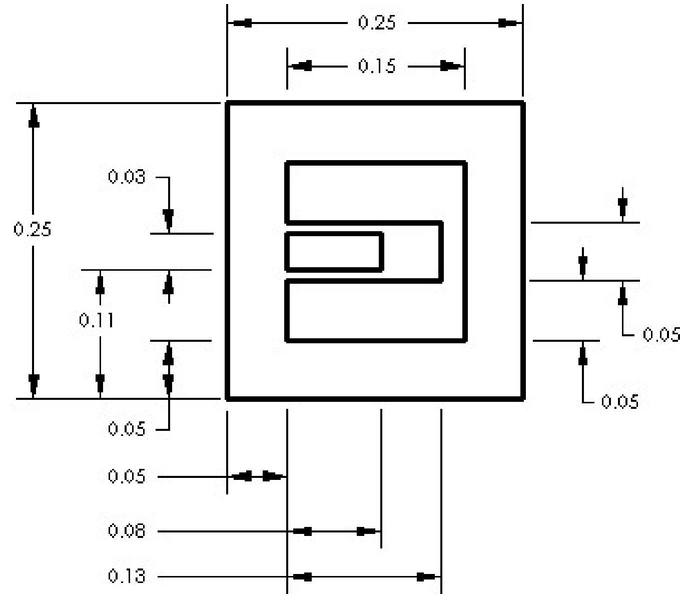

Figure 5. The unit cell geometry for the MEMS mirror design. Dimensions are in millimeters.

We can analyze the deflection and stress characteristics for each of the mirrors in the array of 100 elements by meshing and solving for the single mirror case. Although it is more satisfying to solve the entire structure, this approach is sufficient to find stress concentration issues and deflection characteristics. A single unit assembly is rendered in Figure 6. The underlying silicon exemplifies the characteristic <111> etch plane geometry, where we have chosen an etch depth of 25 mm for this view. Of course, this value, along with others, may be set through the use of a design table at the component level; then one of several configurations may be checked with COSMOS/Works to perform a variational analysis over several parameter spaces.

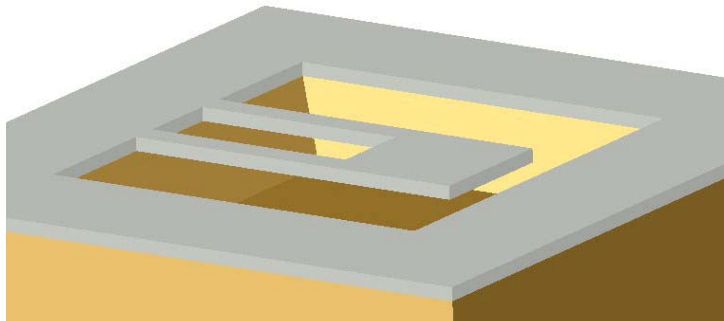

Figure 6. Rendered model of the unit MEMS assembly.

Deflection Analysis

By setting up a design table for the Base component, we have established a technique for evaluating mirror deflection as a function of applied voltage and etch depth of the silicon well. <100> silicon wafers, etched as described above, will exhibit flat terminal planes, parallel to the wafer surface. The design table employed for this deflection analysis initially used depths of 10 µm and 5 µm. In the assembly document, configurations were defined using each of the etch depth component designs from the design table.

The COSMOS/Works deflection analysis of a 10 µm etch depth indicated a maximum deflection of only 9nm at 50 V. Figure 7 is a direct output from the COSMOS/Works analysis tool, where the apparent deflection (shown in the figure) is scaled by a factor of 400. The Coulomb force of

attraction responsible for moving the mirror is quadratic in voltage and follows an inverse square law *vs.* electrode separation. So half the separation between electrodes would imply four times the deflection. Appendix A details the closed-form relations that were used to approximate the static deflection of the cantilevered beam under voltage application. In this example, we solved for the "zero-deflection" force and assumed minimal change in force at the furthest extent of mirror travel. We also ignored the shape of the mirror element as it bends (slightly) while deflecting.

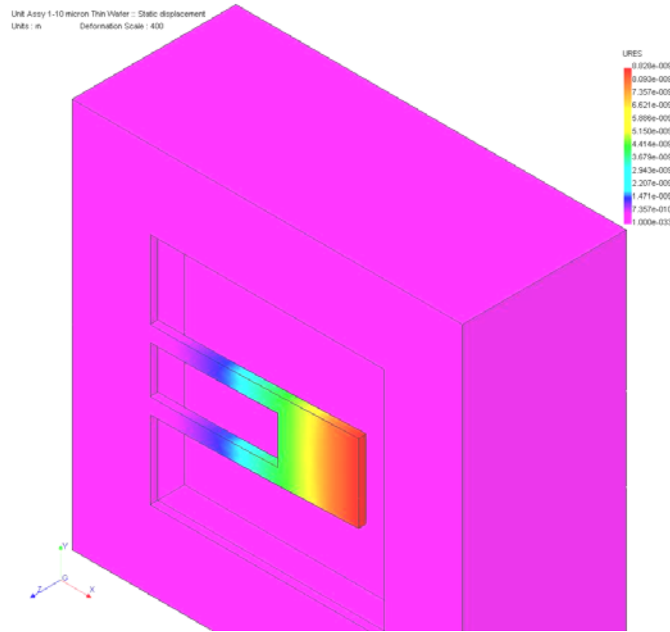

Figure 7. Deflection map for a 5 μm thick Ni film at 50 V, 10 μm etch depth.

The simplifications mentioned above could result in very poor estimation of actual behavior in cases where the deflection is a large fraction of the gap dimension. Furthermore, one should evaluate the response of the un-actuated cantilever under severe shock-loading to ensure the device will withstand shipping and moderate mishandling. We are treating such concerns as beyond the scope of this brief study, but in the real world of product reliability and the need for optimal modeling competence these considerations must be explored. COSMOS/EMS may be used to evaluate the finite difference modeling needed to solve for deflection when one electrode is moving and changing shape.

As for the shock-load characteristics, mass analysis of the structures will allow setting up a force that equals, say, a 500 g force spike. This force may then be applied to the model to predict the resulting maximum deflection.

Another entry in the design table and configuration manager for nickel thickness allows us to evaluate the effect of using a thinner nickel film. Table 1 summarizes the results of several configurations, where we have included the stress analysis results, too. The stress numbers are available from each design study, so we chronicle them during the hunt for appropriate deflection values.

Table 1. Four element design study of deflection, stress, and strain *vs.* etch depth and Ni thickness. The yellow-highlighted design parameters produced the desired ~1 micron deflection.

Configuration Name	d (mm)	Wafer Thk (microns)	Ni Thk (microns)	V	F (N)	Max Deflect (microns)	Max Stress (N/m^2)	Strain (m/m)
Thk NI_10 Micron Thin	0.010	100	5	50	5.53E-07	0.009	7.72E+05	2.22E-06
Thk Ni_5 Micron Thin	0.005	100	5	50	2.21E-06	0.035	3.09E+06	8.61E-06
Thin Ni_10 Micron Thin	0.010	100	1	50	5.53E-07	0.912	1.62E+07	4.92E-05
Thin Ni_5 Micron Thin	0.005	100	1	50	2.21E-06	4.000	6.89E+07	2.30E-04

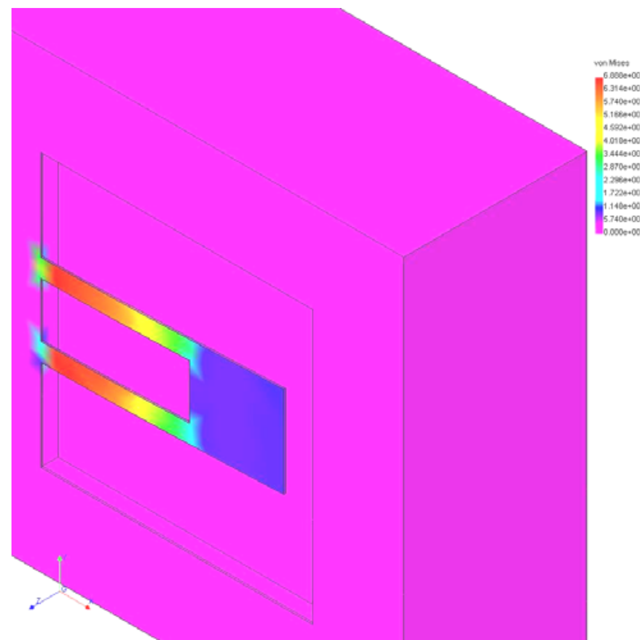

Figure 8. Optimized for displacement of approximately 1 micron at 50V. 10 micron etch depth, 1 micron Ni layer. Displacement result.

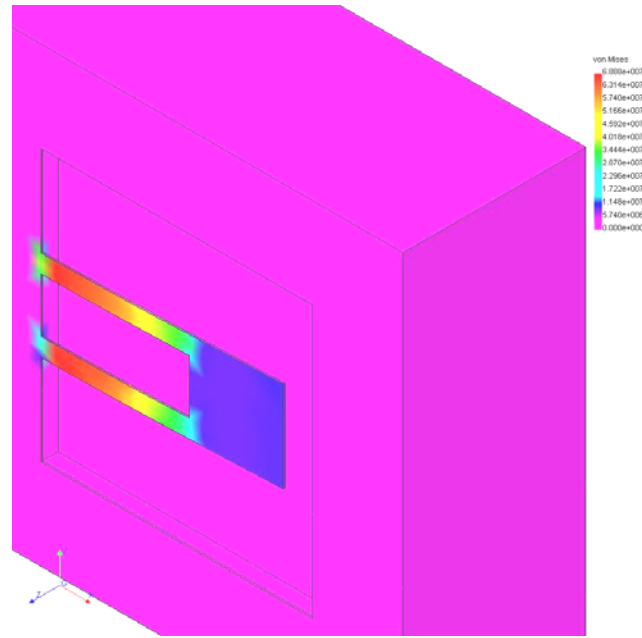

Figure 9. The von Mises stress map for the MEMS device with etch depth 10 microns and 1 micron thick Ni suggests a maximum stress of 1.62 x 10^7 N/m^2. The greatest stress concentration is not right at the anchor point, but tens of microns away.

Appendix A

Calculation of force on plate of a capacitor

One of the possible applications for the MEMS structures described herein is an electrically addressable optical beam deflector. To understand the deflection *vs.* applied voltage characteristics of such a device, we model each mirror as a parallel-plate capacitor, where we ignore the shape change of the cantilever beam as it undergoes deflection. We have also chosen to ignore the decrease in plate separation resulting from deflection, leaving that for future exploration.

For a parallel-plate capacitor, the force F (in Newtons) on one plate for charge Q (Coulombs) and plate area A (square meters), may be expressed[2] as

$$F = \frac{Q^2}{2\varepsilon_0 A} \tag{1}$$

where ε_0 is the permittivity of free space. Since we are only interested in the scalar magnitude of the force in this case, we simplify the nomenclature by evaluating F as the modulus of the force vector, that is,

$$F = \left|\vec{F}\right| \ . \tag{2}$$

For a capacitor charged to V volts, Q is related to the capacitance C by

$$Q = CV \ . \tag{3}$$

Combining Equation 1 with Equation 3, we get

$$F = \frac{C^2 V^2}{2\varepsilon_0 A} \ . \tag{4}$$

To relate the force directly to the physical geometry of the capacitor and the voltage, we utilize the relation

$$C = \varepsilon_0 \frac{A}{d} \tag{5}$$

to arrive at

$$F = \varepsilon_0 \frac{V^2 A}{d^2} \ , \tag{6}$$

where d is the plate separation (in meters).

[1] Parameswaran, M., D. Xie, and P. G. Glavina, "Fabrication of nickel micromechanical structures using a simple low-temperature electroless plating process," J. Electrochem. Soc., **140**, L111-L112 (1993).

[2] R. Feynman, R. Leighton, and M. Sands, The Feynman Lectures on Physics, Addison Wesley, 1989.